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10CS33

Third Semester B.E. Degree Examination, December 2011
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Draw the truth table and explain how a TTL NAND gate works. **(06 Marks)**

b. An asymmetrical signal waveform is high for 2msec and low for 5msec. Find the frequency and the duty cycle L of the waveform. **(04 Marks)**

c. Discuss the positive and negative logic and list the equivalences in positive and negative logic. **(05 Marks)**

d. Draw the timing diagram and write a Verilog HDL code (using structural model) for the Boolean function Y = NAND(Y1, Y2); where Y1 = A + B, Y2 = B + C. **(05 Marks)**

2 a. A digital system is to be designed in which the months of the year is given as input in four bit form. The month January is represented as '0000', February as '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0'. Consider the excess numbers in the input beyond '1011' as don't care conditions. For this system of four variables (A, B, C, D), find the following :

i) Boolean expression in Σm and πM form
ii) Write the truth table
iii) Using K-map, simplify the Boolean expression of canonical min term form
iv) Implement the simplified equation using NAND-NAND gates. **(10 Marks)**

b. Using Q-M method, simplify the expression $f(A, B C, D) = \Sigma(0, 3, 5, 6, 7, 11, 14)$. Write the gate diagram for the simplified equation using NAND-NAND gates. **(10 Marks)**

3 a. Implement the Boolean function expressed by POS, $f(A, B, C, D) = \pi(1, 2, 5, 6, 9, 12)$ using 8-to-1 MUX. **(08 Marks)**

b. Draw a PLA circuit to simultaneously realize the Boolean functions Y3 = A'BC' ; Y2 = AC ; Y1 = AB'C + A'BC + ABC' ; Y0 = A'BC' + A'BC + A'B'C' + ABC. **(06 Marks)**

c. Implement a full adder using a 3-to-8 decoder. **(06 Marks)**

4 a. Draw the logic diagram of clocked 'D' flip-flop. Write its truth table, characteristic equation, state diagram and excitation table. What is the drawback of SR flip-flop? **(10 Marks)**

b. Explain the Schmitt-Trigger transfer characteristic. **(06 Marks)**

c. Using behavioral model, write verilog HDL code for a 'D' flip-flop. **(04 Marks)**

PART – B

5 a. Using negative edge triggered JK flip-flops, draw the logic diagram of a 4-bit serial In - serial Out shift register. Draw the waveform to shift the binary number 1010 into this register. Also, draw the waveforms for four clock transitions when J = K = 0 (assuming the register has stored 1010 in it). **(08 Marks)**

b. How long will it take to shift the hexadecimal number 'AB' into the 54/74164 (SIPO) if 5MHz clock is connected to it? Also, mention the time required to extract an 8-bit number from the same register. **(04 Marks)**

c. With a neat diagram, explain a 4-bit universal shift register. **(05 Marks)**

d. Write Verilog code for switched-tail counter using 'assign' and 'always' statements. **(03 Marks)**

6 a. Mention any two differences between asynchronous and synchronous counter. With a neat block diagram, output waveforms and truth table. Explain a 3-bit binary Ripple Down-Counter constructed using negative-edge trigged JK flip-flops. **(10 Marks)**

b. A 4-bit binary asynchronous counter is connected with a clock of 500 KHz frequency. Find the time period of the waveform at the output of the first and the last JK flipflop. **(02 Marks)**

c. Design a synchronous mod-6 counter using JK flipflop. **(08 Marks)**

7 a. Compare Moore and Mealy model of synchronous sequential circuit. **(06 Marks)**

b. Design an asynchronous sequential logic circuit for state transition diagram shown in Fig.Q7(b).

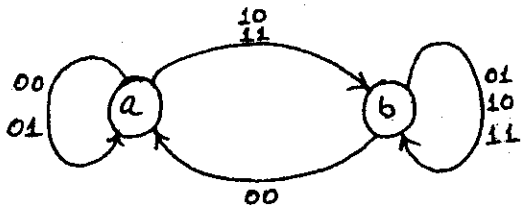

Fig.Q7(b) **(06 Marks)**

c. Reduce state transition diagram (Moore model) of Fig.Q7(c) by,
i) Row elimination method ii) Implication table method. **(08 Marks)**

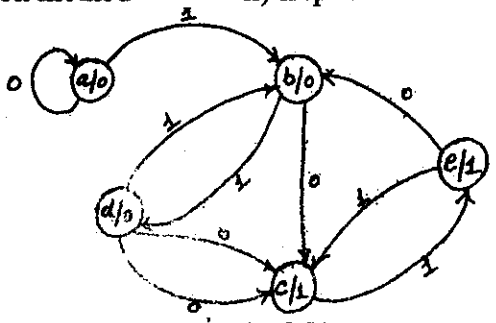

Fig.Q7(c)

8 a. Discuss the two drawbacks of resistive divider used in converting digital input to analog output. Draw the schematic for a 4-bit binary ladder and explain how the digital to analog conversion is achieved using it. **(10 Marks)**

b. Using a schematic block diagram, briefly explain counter type ADC. **(08 Marks)**

c. A counter type 10 bit ADC is connected with 7 MHz clock. Find :
i) The average conversion time
ii) The maximum conversion rate. **(02 Marks)**

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